

1 **MEDIATEK INC.,**2 **Plaintiff,**3 **vs.**4 **FREESCALE SEMICONDUCTOR, INC.,**5 **Defendant.**

6 Case No.: 11-cv-5341 YGR

7 **ORDER GRANTING MEDIATEK'S MOTION**
8 **FOR JUDGMENT OF INFRINGEMENT AS A**
9 **MATTER OF LAW AND DENYING**
10 **FREESCALE'S MOTION FOR JUDGMENT AS A**
11 **MATTER OF LAW**

12 Plaintiff MediaTek Inc. ("MediaTek") moves the Court pursuant to Federal Rule of Civil
13 Procedure 50 for judgment as a matter of law that Defendant Freescale Semiconductor Inc.
14 ("Freescale") has infringed Claims 1, 2, and 5 of U.S. Patent No. 6,738,845 ("the '845 patent"). As
15 grounds for this motion, MediaTek argues that Freescale's sole non-infringement defense depends on
16 an improper claim construction argument of the term "arbitrate among" as used in Claim 1 of the
17 '845 Patent, which presents a question of law reserved for the Court. MediaTek argues that the term
18 "arbitrate among" does not require construction, and that Freescale is attempting to limit the meaning
19 of the term without any basis for doing so.

20 Freescale likewise moves for judgment as a matter of law that the claim term in "arbitrate
21 among at least" in U.S. Patent No. 6,738,845 ('845 patent) be construed to mean "to select from at
22 least all of," and that Freescale has not infringed the '845 patent.

23 The parties agree that there is no factual dispute concerning the relevant structure and
24 operation of the Freescale products accused of infringing Claims 1, 2, and 5 of the '845 Patent.

1 Based upon the arguments and evidence presented in support of and in opposition to the
2 motions, the Court Orders that: (1) Freescale's motion for judgment as a matter of law is **DENIED**;
3 and MediaTek's motion for judgment as a matter of law is **GRANTED** on the issue of liability for
4 literal infringement of Claims 1, 2, and 5 of the '845 Patent by Freescale's i.MX6 products.

5 **I. APPLICABLE STANDARD**

6 Pursuant to Rule 50 of the Federal Rules of Civil Procedure, a court may grant judgment as a
7 matter of law (JMOL) against a party on a claim or issue where the party has been "fully heard on
8 [that] issue during a jury trial," and a "reasonable jury would not have a legally sufficient evidentiary
9 basis" to find for that party. *See Fed. R. Civ. P. 50(a)-(b); see also Mformation Techs., Inc. v.*
10 *Research in Motion Ltd.*, No. 08-04990, 2012 WL 3222237, at *1 (N.D. Cal. Aug. 8, 2012) ("A party
11 is entitled to judgment as a matter of law if, under the governing law, there can be but one reasonable
12 conclusion as to the verdict, and that is a finding in favor of the moving party.") (citing *Winarto v.*
13 *Toshiba Am. Elecs. Components, Inc.*, 274 F.3d 1276, 1283 (9th Cir. 2001)). In reviewing a JMOL
14 motion, the Court must draw all reasonable inferences in favor of the nonmoving party, and
15 determine whether reasonable minds could come to a single conclusion in favor of the moving party.
16 *See E.E.O.C. v. Go Daddy Software, Inc.*, 581 F.3d 951, 961 (9th Cir. 2009).

17 **II. CLAIM CONSTRUCTION – "ARBITRATE AMONG"**

18 The '845 Patent, Claim 1 reads:

19 1. A system, comprising:
20 a first data processing subsystem comprising a first processor coupled to a first bus as a
21 first bus master;
22 a second data processing subsystem comprising a second processor coupled to a second
23 bus as a second bus master;
24 a direct memory access (DMA) subsystem comprising a DMA controller coupled to a
25 third bus as a third bus master;
26 a first slave subsystem comprising a memory unit coupled to a fourth bus;
27 a second slave subsystem comprising a fifth bus;
28 *a first arbitration unit associated with the first slave subsystem, having each of the first,*
 second, third and fourth busses coupled thereto, configured and arranged to
 arbitrate among at least the first data processing subsystem, the second data
 processing subsystem, and the DMA subsystem for access to the first slave
 subsystem, and to couple the fourth bus to any selected one of at least the first,

1 *second, and third busses so as to enable a selected one of at least the first data*
2 *processing subsystem, the second data processing subsystem, and the DMA*
3 *subsystem to access the first slave subsystem; and*
4 a second arbitration unit associated with the second slave subsystem, having each of the
5 first, second, third and fifth busses coupled thereto, configured and arranged to
6 arbitrate among at least the first data processing subsystem, the second data
7 processing subsystem, and the DMA subsystem for access to the second slave
8 subsystem, and to couple the fifth bus to any selected one of at least the first,
9 second, and third busses so as to enable a selected one of at least the first data
10 processing subsystem, the second data processing subsystem, and the DMA
11 subsystem to access the second slave subsystem
12 *wherein each of the first and second arbitration units is configured and arranged to*
13 *operate independently such [that] the first arbitration unit can enable any[]one of*
14 *the first data processing subsystem, the second data processing subsystem, and the*
15 *DMA subsystem to access the first slave subsystem at the same time that the*
16 *second arbitration unit enables any other of the first data processing subsystem,*
17 *the second data processing subsystem, and the DMA subsystem to access the*
18 *second slave subsystem; and*
19 *wherein the DMA subsystem is configured and arranged such that, when the first and*
20 *second arbitration units enables the DMA subsystem to access each of the first and*
21 *second slave subsystems, the DMA controller can cause data to be transferred*
22 *between the first slave subsystem and the second slave subsystem via the third bus.*

(Emphasis supplied.)

In its prior motion for summary judgment on this issue,¹ and during the course of the trial, Freescale has argued that the “arbitrate among” term must mean that the “first arbitration unit” is configured and arranged to receive requests from all three of the master components (the first data processing subsystem, the second data processing subsystem, and the DMA subsystem) for access to the first slave subsystem simultaneously. In the instant motion for judgment as a matter of law, Freescale’s argument as to the meaning of the claim language has been revised slightly to contend

¹ Defendant Freescale previously moved for summary judgment on MediaTek’s claims that Freescale’s i.MX6 family of chips infringe Claims 1, 2, and 5 of the ‘845 Patent. In the i.MX6 products, the accused arbitration unit does not select between two separate data processing subsystems and a DMA subsystem at the same time. Instead, requests from the two data processing subsystems are arbitrated by another arbiter before they reach the alleged “first arbitration unit.” Thus, Freescale argued that its i.MX6 family of chips does not infringe asserted Claims 1, 2, and 5 of the ’845 patent because they do not arbitrate “among at least the first data processing subsystem, the second data processing subsystem, and the DMA subsystem for access to the first slave subsystem,” at the same time. The Court denied that motion, finding that Freescale was using a definition of “among” that was limited inconsistent with the intrinsic evidence. (Dkt. No. 554.)

1 that the “first arbitration unit” must be presented and be able to select from among all three masters’
2 requests at one time. Freescale argues that the surrounding language of Claim 1, the language of
3 other claims in the patent, the specification, and the prior art all support this understanding of
4 “arbitrate among.”

5 The Court finds that the meaning of “arbitrate among” is not limited in the ways that
6 Freescale suggests. Nothing in the language of Claim 1 requires that requests from each of the
7 masters be presented directly or simultaneously to the “first arbitration unit.” Rather, the language of
8 Claim 1 provides that the “first arbitration unit” be “configured and arranged to arbitrate among”
9 requests from the three masters “for access to the first slave subsystem,” and to couple the fourth bus
10 to that “selected one of” the three masters to access the first slave subsystem. That is, the first
11 arbitration unit must be capable of providing access to the first slave subsystem in response to a
12 request from any of the three masters via the fourth bus. Thus, this claim language does not preclude
13 a device where an intervening module filters out one request before it reaches the “first arbitration
14 unit,” so long as the “first arbitration unit” could enable a request from any one of the three to access
15 the “first slave subsystem.” In other words, the “arbitrate among” language requires simply that the
16 arbiter select one of the masters for access to the first slave subsystem and that the selected one could
17 be any of the three masters. The literal terms require no more.

18 The surrounding language of Claim 1 does not change this analysis. The first “wherein”
19 clause states that the “first arbitration unit” and “second arbitration unit” are “configured and
20 arranged to operate *independently* such [that] the first arbitration unit can enable any [] one of the”
21 three masters to access the first slave subsystem “at the same time that the second arbitration unit
22 enables any other of” the three masters to access the second slave subsystem. Freescale argues that
23 the requirement to operate “independently” means that the “first arbitration unit” must function
24 without any input from the “second arbitration unit.” The Court, in its *Markman* Order, determined
25 that the “wherein” clause’s “configured and arranged to operate independently” language meant that
26 the two arbitration units must be “configured and arranged to operate without regard to the other
27 arbitration unit.” (Dkt. No. 127 at 17.) At the same time, the Court rejected Freescale’s argument
28 that, in order for the arbitration units to “operate independently” they must operate “without reliance

1 or dependence,” since different parts of system could “rely” on each other while still operating “at
2 the same time” and “without blocking” one another. (*Id.* at 13-14.) Thus, the requirement that the
3 two arbitration units “operate independently” does not lead to the conclusion that the “first
4 arbitration unit” must be configured and arranged to each receive requests simultaneously from all
5 three masters.² The literal language of the claim allows for arbitration units which operate at the
6 same time, without blocking one another, but which also pass on a request from one unit to another.

7 Freescale’s claim differentiation argument also fails. Claims 23 and 24 depend from Claim
8 21, not Claim 1, and concern a different system with different requirements. *See RF Delaware, Inc.*
9 v. *Pac. Keystone Techs., Inc.*, 326 F.3d 1255, 1263 (Fed. Cir. 2003) (“Although claim differentiation
10 is not a hard and fast rule of construction, it is applicable where there is a dispute over whether a
11 limitation found in a dependent claim should be read into an independent claim, and that limitation is
12 the only meaningful difference between the two claims.”). Moreover, Freescale’s argument that
13 “arbitrate” requires “active selection” between requests presented to the arbiter roams far afield of
14 the actual language of the patent.³

15 Likewise, Figure 3 of the specification does not support a requirement that the “first
16 arbitration unit” receive requests from all three masters at the same time. The ‘845 Patent’s
17 specification, which repeatedly and consistently states that the components disclosed in the figures
18 are exemplary or “illustrative embodiments,” cannot be used to create a limit in the scope of the
19 claim language where none exists. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005);
20 *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1358 (Fed.Cir.2004) (“Absent a clear
21 disavowal or contrary definition in the specification or the prosecution history, the patentee is

22

23 ² Indeed, the fact that the first “wherein” clause uses the words “at the same time” to
24 describe the operation of the arbitration units in relation to one another, but does not use similar
25 language to describe the how “first arbitration unit” selects between requests from the three masters,
term.

26 ³ The Court notes that Claims 23 and 24 include “at the same time” language not present in
27 the description of how the “first arbitration unit” is to “arbitrate among” requests from the three
masters.

1 entitled to the full scope of its claim language.”); *Linear Tech. Corp. v. Int'l Trade Comm'n*, 566 F.3d
2 1049, 1055 (Fed. Cir. 2009) (refusing to narrow scope of claim language based up on specification).

3 Finally, Freescale argues that the prosecution history of the ‘845 Patent supports its
4 construction of “arbitrate among.” In order to distinguish a prior art reference (So), during the
5 course of patent prosecution, the patentee amended Claim 1 to replace a single “bus arbitration
6 module” with two bus arbitration units, each unit associated with a single slave subsystem. The
7 inventors stated in that amendment the following requirement of claim 1:

8 *Claim 1 requires each of two different arbitration units to arbitrate among a first data
9 processing subsystem, a second data processing subsystem, and a DMA subsystem for access
10 to a respective slave subsystem associated with it. Such an architecture is not disclosed or
suggested by So.*

11 (‘845 prosecution history, Dec. 12, 2003 Amendment, at 14.) The language that was offered to
12 distinguish patentably over the So reference—including a “DMA controller interrelated with a first
13 and second arbitration unit,” and “each of two different arbitration units to arbitrate among a first
14 data processing subsystem, a second data processing subsystem, and a DMA subsystem for access to
15 a respective slave subsystem associated with it”—does nothing to establish the limitation
16 (simultaneous, or selecting from all three at the same time) that Freescale proposes. As any
17 disavowal of the full scope of the claim language based upon the prosecution history must be “clear
18 and unambiguous,” *see Phillips*, 415 F.3d at 1317; *Storage Tech.*, 329 F.3d at 833-34, this argument
19 does not aid Freescale’s claim interpretation.

20 III. LITERAL INFRINGEMENT

21 At trial, MediaTek’s technical expert, Dr. Krste Asanović, testified that Freescale infringes
22 claims 1, 2, and 5 based on Freescale’s i.MX6DQ and i.MX6SDL processors (collectively, the
23 “i.MX6 products”). In support of that infringement opinion, Dr. Asanović testified in detail about the
24 relevant structure and operation of the i.MX6 products. Specifically, the i.MX6 products include a
25 bus interconnect called a NIC-301 that includes individual arbitration components. Both of these
26 arbitration units connect multiple bus masters to multiple bus slaves, including the OCRAM and the
27 MMDC. Dr. Asanović also explained to the jury how these components of the i.MX6 products meet

1 each and every limitation of claim 1. (Trial Tr. at 699-715.) He identified: (1) the ARM platform
2 (shown in green above) coupled to two AXI busses as the “first data processing subsystem” (*id.* at
3 703:20-25); (2) the IPU-1 (shown in blue) coupled to a bus as the “second data processing
4 subsystem” (*id.* at 704:19-705:3); and (3) the SDMA (shown in blue) coupled to a pair of busses as
5 the “direct memory access (DMA) subsystem” (*id.* at 705:18-20). Dr. Asanović further explained
6 that the OCRAM and bus that connects it to the slave port of one arbitration unit together satisfy the
7 “first slave subsystem” limitation (*id.* at 706:10- 12), and that an external memory controller called
8 the MMDC and a pair of busses that connect the MMDC to the slave port of another arbitration unit
9 meet the “second slave subsystem” limitation (*id.* at 707:3-21). Dr. Asanovic also testified to his
10 bases for concluding that these same i.MX6 products infringe dependent claims 2 and 5. (*Id.* at
11 716:2-717:3.)

12 Again, there is no dispute about these facts concerning the structure and operation of the
13 accused chips. The Court finds no basis for reading a requirement that the first arbitration unit be
14 configured and arranged to select from all three of the ARM, IPU, and SDMA at the same time, and
15 this is the only non-infringement argument offered by Freescale with respect to Claims 1, 2, and 5 of
16 the ‘845 Patent. As a consequence, the Court finds, as a matter of law, that the accused i.MX6
17 products literally are covered by each and every limitation of Claims 1, 2, and 5 of the ‘845 Patent.

18 **IV. CONCLUSION**

19 Based upon the foregoing, Freescale’s motion for judgment as a matter of law is **DENIED**.
20 MediaTek’s motion for judgment as a matter of law is **GRANTED** as to liability for direct
21 infringement of Claims 1, 2, and 5 of the ‘845 Patent by Freescale’s i.MX6 products. The matter of
22 damages remains one for the jury.

23 This order terminates the motions at Docket Nos. 659 and 660.

24 **IT IS SO ORDERED.**

25 Dated: September 17, 2014

26 
27 YVONNE GONZALEZ ROGERS
28 UNITED STATES DISTRICT COURT JUDGE